REMARKS

Claims 6-25, 28, 30, 34-37 and 40 are pending in this application. By this Amendment, claims 6, 16, 17, 21, 23, 25, 30, 35 and 40 are amended and claim 33 is cancelled without prejudice or disclaimer. Various amendments are made for clarity and are unrelated to issues of patentability.

Applicants gratefully acknowledge the Office Action's indication that claims 21-24, 30 and 39 are allowed. By this Amendment, allowable features of dependent claim 39 are incorporated into independent claim 35. Thus, independent claim 35 defines patentable subject matter. Additionally, for at least the reasons set forth below, all claims are believed to be allowable.

The Office Action rejects claims 6-9, 14-17, 19-20, 25, 27-28, 32-37 and 40 under 35 U.S.C. §103(a) over U.S. Patent Publication 2004/0100994 to Miller, U.S. Patent 7,047,385 to Bhattacharya et al. (hereafter Bhattacharya) and U.S. Patent 6,732,247 to Berg et al. (hereafter Berg). The Office Action also rejects claim 10 under 35 U.S.C. §103(a) over Miller, Bhattacharya and U.S. Patent Publication 2002/0156995 to Martin et al. (hereafter Martin). Still further, the Office Action rejects claim 11 under 35 U.S.C. §103(a) over Miller, Bhattacharya, Berg and U.S. Patent Publication 2003/0037226 to Tsuruta et al. (hereafter Tsuruta). The Office Action rejects claims 12-13 over 35 U.S.C. §103(a) over Miller, Bhattacharya, Berg and U.S. Patent No. 6,052,802 to Zahir et al. (hereafter Zahir). The Office Action also rejects claim 18 under 35 U.S.C. §103(a) over Miller, Bhattacharya, Berg and Potter. The rejections are respectfully traversed with respect to the pending claims.

Independent claim 6 recites a plurality of systolic memory arrays each divided into banks, each of the memory arrays arranged in a pipelined architecture and each of the plurality of systolic memory arrays to support pipeline access to the corresponding banks using a plurality of data pipes. Independent claim 6 also recites a plurality of pipeline registers, each register to couple to a first one of the banks of a corresponding one of the plurality of systolic memory arrays to provide read and write operations through a data pipe to the banks of the corresponding one of the systolic memory arrays beginning with the first one of the banks and to provide address access through an address pipe to the banks of the corresponding one of the systolic memory arrays beginning with the first one of the banks.

The applied references do not teach or suggest all the features of independent claim 6. More specifically, the Office Action relies on Bhattacharya as disclosing multiple arrays of memory banks and relies on Berg as disclosing pipeline registers. However, the combination of Miller, Bhattacharya and Berg does not teach or suggest the specific features relating to the systolic memory arrays each divided into banks and the claimed plurality of pipeline registers.

More specifically, Bhattacharya merely discloses memory banks that may be addressed on an address bus 15 and may be coupled to read/write buses 12 and 14 by data selectors 16. See Fig. 1A of Bhattacharya. Each memory bank may have a data input, a data output and an address input. See col. 6, lines 39-42. See also col. 1, lines 47-58 discussing that the address input is provided from the address pipeline (i.e., the address

bus 15) and data read from the memory blocks is provided from the data pipeline (i.e., busses 12, 14).

Berg discloses a plurality of memory banks 40 coupled together on a bus with pipeline registers 44 at regular intervals. See Fig. 3 and col. 3, lines 49-59. The memory banks 0, 1, 2, 3 form a first pipeline 48 and the memory banks 4, 5, 6 and 7 form a second pipeline 50. Accordingly, Berg teaches that pipeline registers 44 are provided at intervals along a pipeline in which the pipeline is in a form of a ring. There is no suggestion of how Berg's pipelines 48/50 (that include a plurality of memory banks and registers) may be provided within Bhattacharya's Fig. 1A configuration that utilizes an address bus 15 and data buses 12 and 14. In other words, there is no suggestion of how Berg's registers 44 may be provided within Bhattacharya's Figure 1A.

In Berg, data flows in accordance with the arrows of the pipelines 48 and 50. Therefore, data flows in through one memory bank and out of another memory bank. This clearly differs with data flow and address flow in Bhattacharya's Fig. 1A. Thus, the applied references (including Berg) do not teach or suggest a plurality of pipeline registers, each register to couple to a first one of the banks (arranged in the pipeline architecture) of a corresponding one of a plurality of systolic memory arrays to provide read and write operations through a data pipe to the banks of the corresponding one of the systolic memory arrays beginning with the first one of the banks and to provide address access through an address pipe to the banks of the corresponding one of the systolic memory arrays beginning with the first one of the banks. Accordingly, the combination of Miller, Bhattacharya and Berg does not teach or suggest all the features of independent claim 6.

The other applied references do not teach or suggest the missing features of independent claim 6. Thus, independent claim 6 defines patentable subject matter.

Independent claim 16 recites a plurality of systolic memory arrays each divided into banks, each of the systolic memory arrays arranged in a pipelined architecture and each of the plurality of memory arrays to support pipeline access to the corresponding banks using a plurality of data pipes, and a writing operation into the memory is performed by pumping an address with data that is to be written into the memory. Independent claim 16 also recites a plurality of pipeline registers, each register to couple to a first one of the banks of a corresponding one of the plurality of systolic memory arrays through a data pipe and an address pipe to provide read/write data input, data output and address access to the banks of the corresponding one of the systolic memory arrays through the first one of the banks arranged in the pipelined architecture.

For at least similar reasons as set forth above, the applied references do not teach or suggest all the features of independent claim 16. Thus, independent claim 16 defines patentable subject matter.

Independent claim 25 recites that the systolic memory includes a plurality of separate systolic memory arrays, each systolic memory array including a plurality of memory banks in a pipelined fashion, the plurality of memory banks of each systolic memory array to share an address line in a pipelined fashion and data lines in a pipelined fashion, and a read operation from the systolic memory is performed by pumping an address once and allowing the address to flow through an address pipe to reach individual banks one cycle at a time. Independent claim 25 also recites that the systolic memory

includes a plurality of pipeline registers, each register coupled to one of the separate systolic memory arrays, and each register is coupled to one end of a corresponding one of the systolic memory arrays to provide read data from the memory array, to provide write data to the array and to provide address information to the array. For at least similar reasons as set forth above, the applied references do not teach or suggest all the features of independent claim 25. Thus, independent claim 25 defines patentable subject matter.

Independent claim 40 recites a plurality of separate systolic memory arrays, each systolic memory array including a plurality of memory banks in pipelined fashion, the plurality of memory banks of each systolic memory array to share an address line in a pipelined fashion and data lines in a pipelined fashion, and peripheral access for writing operations and addressing for one systolic memory array is accomplished from one side of the one systolic memory array and data for reading operations for the one systolic memory array is received from the one side of the one systolic memory array.

For at least similar reasons as set forth above, the applied references do not teach or suggest all the features of independent claim 40. Thus, independent claim 40 defines patentable subject matter.

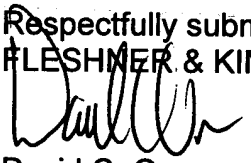
For at least the reasons set forth below, each of independent claims 6, 16, 25, 35 and 40 define patentable subject matter. Each of the dependent claims depends from one of the independent claims and therefore defines patentable subject matter at least for this reason. In addition, the dependent claims recite features that further and independently distinguish over the applied references.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance of claims 6-25, 28, 30, 34-37 and 40 are earnestly solicited. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
FLESHNER & KIM, LLP



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Date: December 29, 2006